REMARKS

Claims 22-39 were pending in the application for reconsideration. In response to the office action, applicants have added new claims 40-42. Claims 22-42 are now pending for reconsideration.

Claims 22-39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Selvidge (U.S. Patent No. 5,649,176) in view of Dargelas (U.S. Patent No. 5,938,753). Applicants respectfully traverse this rejection for the following reasons.

MPEP § 706.02(j) sets forth the required contents of a 35 U.S.C. 103 rejection. In pertinent part, MPEP § 706.02(j) indicates that "[a]fter indicating that the rejection is under 35 U.S.C. 103, the examiner should set forth in the Office action:

(A) the relevant teachings of the prior art relied upon."

The office action fails to meet this requirement of MPEP § 706.02(j) because the office action mischaracterizes the allegedly relevant teachings of the prior art relied upon. In particular, the office action asserts that Selvidge discloses "providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit (virtual clock VClk in Fig. 16B; and column 18, lines 58-65)." This is a factually inaccurate statement of the teachings of Selvidge. As a purely factual matter, col. 18, lines 58-65 of Selvidge state:

> . . . An example is shown in Fig. 16A, this implicit state can be transformed into an explicit state element which is clocked by the virtual clock VClk by simply choosing a wire 1601 in the loop and inserting a flip-flop 1602 which is clocked by the virtual clock VClk as shown in Fig. 16B.
> The addition of flip-flop 2602 [sic] changes the timing characteristics of the loop. . . .

The office action also mischaracterizes the allegedly relevant teachings of Dargelas. In particular the office action asserts that Dargelas discloses "generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element

(Dargelas, Abstract)." This is a factually inaccurate statement of the teachings of Dargelas. As a purely factual matter, the Abstract of Dargelas states:

> A method and computer system for automatically determining test patterns for a netlist having multiple clocks and sequential circuits. The invention utilizes a static model of a sequential circuit and models the sequential circuit having multiple clock signals (e.g., one model is used for all multiple clock signals). The multiple clock signals include primary clock input signals and internal clock signals. The clock signals can be gated or dual edge. The invention makes use of the "iterative array representation of sequential circuits" (IAR) model for automatic test pattern generation (ATPG) but utilizes a static sequential circuit model. The invention receives user defined input clock signal waveforms and determines a cycle of clocks based thereon that statically represents all waveforms over time. The cycle of clocks is divided into frames where each frame contains stable clock values. The stable clock values are used to determine the values of each signal that clocks a sequential circuit of the netlist for each frame. This information is then used to determine which sequential circuits are active and which are not active for any given frame. The IAR model is then given the active/inactive information and the ATPG process uses this information to prune efficiency in the search space and search time for finding test patterns that can distinguish a particular fault. Unlike conventional ATPG processes, test pattern determination efficiency is gained in the present invention by having, in advance, the input clock signals given by the user.

The office action appears to be conflating identification of the allegedly relevant teachings with the Examiner's reasoning and / or analysis of how the allegedly relevant teachings read on the claims. However, this obscures the Examiner's position because it is unclear as to whether the Examiner actually believes that the relied upon portions disclose what is stated in the rejection or whether the Examiner is applying some abstraction or line of reasoning to arrive at such conclusion. As noted in MPEP § 706.02(j), "[i]t is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply." As prosecution of the present application has already be re-opened following appeal (and may be headed back to appeal), it is incumbent upon the Examiner to set forth a full and complete basis of the rejection.

For example, applicants note that the cited portion of Selvidge does not explicitly disclose a "virtual delay element," but the Examiner appears to be relying upon the flip-flop1602 as corresponding to the recited virtual delay element. An example of a more accurate statement of the rejection which may clarify issues for appeal might take the following form:

> Selvidge discloses a flip-flop 1602 which is clocked by a virtual clock VClk (col. 18, lines 58-63). This may be considered to read on the recited providing a virtual clock signal to the virtual delay element.

Applicants submit that if the Examiner followed this approach for each and every claim recitation, it would become apparent that the rejection is erroneous. Applicants respectfully request such a full and complete analysis at least with respect to each contested claim recitation, including, for example, the recited "to influence a desired race condition." The Examiner appears to admit that the relied upon portion lacks such a teaching because in the response to applicants' arguments the Examiner relies on other portions of Selvidge. Applicants note that the Examiner's response to applicants' arguments does not form any part of the rejection of record. The full basis for the rejection must be positively set forth in the statement of the rejection. Again, in order to clarify and simplify issues for appeal, applicants respectfully request that the Examiner perform a full and complete analysis setting forth the full and complete basis in the statement of the rejection, so that the issues may be identified and applicant is provided a fair opportunity to reply.

With respect to claims 22, 28, and 34:

Each of the independent claims 22, 28, and 34 recite features relating to:

generating a netlist model for a circuit;

providing a virtual delay element in the netlist model;

providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and

generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.

By way of background, the invention as presently claimed is directed to the problem of test pattern generation for a circuit which may have a race condition which requires race resolution in order to generate a valid test pattern. None of the cited references are directed to this problem. In fact, Dargelas fails to even mention race resolution and Selvidge mentions race conditions only tangentially in terms of hold time violations.

MPEP § 706.02(j) lists the basic criteria required to establish a prima facie case of obviousness. Among other things, the prior art references when combined must teach or suggest all of the claim limitations. As noted above, the independent claims each recite features related to providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit. The rejection of record continues to fail to give full consideration to each element of this claim recitation. The office action asserts that Selvidge discloses this recitation at col. 18, lines 58-65. This is factually incorrect as is evidenced by simply reading the reproduced portion above. Moreover, this is analytically incorrect.

Selvidge discloses providing a virtual clock to a flip-flop to transform an implicit state into an explicit state element. In the cited portion, the flip-flop 1602 does not appear to correspond to a delay element, virtual or otherwise. Rather, the flip-flop 1602 may more fairly be considered to be a state control element. Nothing in the cited portion of Selvidge suggests that the flip-flop 1602 is inserted to add delay to the circuit. Rather, the purpose of the flip-flop 1602 as explicitly stated is to transform an implicit state into an explicit state element. Moreover, the cited portion is silent with respect to influencing a desired race resolution for the circuit.

In numbered paragraph 6-3, the office action expands on the Examiner's position, citing an out-of-context general statement from the Summary of the Invention and a portion of the Background section, both in col. 2 of Selvidge. It is not apparent that the cited portions of col. 2 have anything whatsoever to do with the relied upon portion at

col. 18 of Selvidge. The Examiner asserts in paragraph 6-3 that "Selvidge's providing a virtual clock to a flip-flop to transform an implicit state into an explicit state is seeking to overcome the hold time problems, i.e., race resolution." Applicants note that this assertion is not supported by the text of Selvidge. The cited portion is silent with respect to both hold time problems and resolving race conditions. In fact, Selvidge teaches that inserting the flip-flop 1602 into the circuit introduces timing concerns, which need to be resolved by adding clock cycles. See Selvidge at col. 18, line 65 through col. 19, line 9.

By way of background, some embodiments of the invention provide flexibility in modeling asynchronous circuits because specific delay conditions may be imposed in specific situations to provide a desired race resolution. For example, page 6, line 27 through page 7, line 5 of the present specification states:

> Through virtual delay elements 24 and 26, a user may impose a specific race resolution through virtual clocks that have timing characteristics that are controlled as virtual primary inputs. For example, if in digital circuit 1, data traveling on second conductive path 12 takes a long time relative to data traveling on first conductive path 8, then a rising edge of vclk2 may be set at a later time than a rising edge of vclk1 to resolve the race. It is in this manner that a user may impose an order as to which set of data arrives at the inputs of OR gate 6 first.

From the foregoing it is clear that in some embodiments the recited providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit involves a flexibility in setting a particular virtual signal to influence a particular desired race resolution. Advantageously, the otherwise asynchronous nature of the circuit may remain while testing of the circuit is simplified.

In contrast to the present invention, Selvidge deals with the problem of asynchronous circuits by transforming the asynchronous circuits into synchronous circuits (see Selvidge Abstract, last sentence). Selvidge then uses the virtual clock to internally clock the now synchronous circuits at a much higher rate (e.g. at least ten times higher than the external clock signal, see Selvidge Abstract). Selvidge controls the propagation of signals by dividing the clock signal into smaller time slices, "in effect

discretizing time and space into manageable pieces" (see col. 2, lines 57-58 of Selvidge). Selvidge addresses hold time violations because a signal with a potential hold time violation would propagate during the initial virtual sub-clock, while the remaining signals would then have ten or more additional sub-clocks to reach the correct value before the next true clock signal. However, the virtual clock of Selvidge is simply a fixed frequency clock (e.g. see Fig. 4B of Selvidge and related description at col. 8, lines 6-15). In other words, the virtual clock of Selvidge is provided indiscriminately to all of the circuit elements and is not provided to any particular element to influence any particular timing issue.

Because Selvidge fails to teach or suggest providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit, the Examiner has failed to establish a prima facie case of obviousness, and each of claims 22, 28, and 34 are patentable over Selvidge in view of Dargelas.

The office action fails to establish a prima facie case for at least the following additional reason. Each of claims 22, 28, and 34 recite features related to generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. The office action admits that Selvidge fails to teach or suggest these recitations and relies on Dargelas for this missing teaching. However, Dargelas fails to make up for the admitted deficiency in Selvidge.

As noted above, the office action asserts that the abstract of Dargelas discloses "generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element." This is factually inaccurate as is evidenced by a review of the abstract of Dargelas (reproduced above). As has been previously pointed out and as remains unrefuted, Dargelas makes no mention of virtual delay elements or virtual clocks. In the absence of a factually accurate statement of the relevant teachings of Dargelas, the Examiner has failed to establish a prima facie case of obviousness.

In numbered paragraph 6-4, the Examiner incorrectly asserts that applicants are arguing the references individually. In fact, applicants are properly attacking the failed combination and the Examiner's failure to establish a prima facie case of obviousness. As noted above, MPEP § 706.02(j) identifies a basic criteria of establishing a prima facie case of obviousness requires that the prior art references when combined must teach or suggest all of the claim limitations. It is a basic tenet of the law of obviousness that if a claim recites elements A, B, C, and D, and none of cited references teaches element D, then the combination of the references cannot possibly teach or suggest the claimed invention of elements A, B, C, and D. The Examiner has admitted that the Selvidge reference fails to teach or suggests the noted claim recitations and has not identified any portion of Dargelas which in fact teaches or suggests the noted claim recitations (the abstract certainly fails to do so). Therefore, no possible combination of Selvidge and Dargelas can render claims 22, 28, or 34 obvious because the admittedly missing claim element is not taught or suggested by the combination. Accordingly, the office action fails to establish a prima facie case of obviousness for this further reason.

The office action fails to establish a prima facie case of obviousness for at least the following additional reason. MPEP § 706.02(j) identifies a basic criteria of establishing a prima facie case of obviousness requires that there must be some suggestion or motivation to modify the reference or combine reference teachings. The suggestion of the combination must be found in the prior art and not based on applicants' disclosure. The Examiner has failed to establish any proper motivation to combine Selvidge and Dargelas in the manner proposed.

Applicants first note that Selvidge is directed to the physical construction of an FPGA. The fields of logic simulation and FPGA configuration are completely different disciplines as compared to automatic test pattern generation. Applicants note that both the US and international classifications of the two patents are different. Accordingly, Selvidge and Dargelas are non-analogous art and one of ordinary skill in the art would not look to the teachings of Dargelas to modify Selvidge.

In any event, the proposed modification is unworkable. The office action relies on col. 1, lines 30-40 as evidence that Selvidge discloses testing a logic design. However, col. 1, lines 30-40 describe some background prior art system and not the system relied upon for allegedly teaching the claim recitations. It is unclear as to what the Examiner is proposing to modify, some background prior art system described in col. 1, lines 30-40 or the virtual clock system described elsewhere in Selvidge. It appears that the Examiner is impermissibly using the claim as blueprint to pick and choose unrelated portions of the references.

Moreover, in substance the Examiner asserts that Dargelas discloses generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. Although not explicitly stated, it appears that the Examiner is relying on Dargelas only for the teaching of generating a test pattern and continues to rely on Selvidge for allegedly teaching the virtual clock signal for the virtual delay element. However, one of ordinary skill in the art would not be motivated to generate a test pattern for the virtual clock signal of Selvidge because Selvidge explicitly discloses that the virtual clock signal is "invisible to the environment" (see Selvidge, Abstract). The fact that Selvidge describes its virtual clock signal as being invisible to the environment teaches away from using the virtual clock signal as a clock input for the system described in Dargelas.

Because Selvidge is non-analogous art with Dargelas, because the Examiner has proposed an unworkable modification, and because Selvidge teaches away from using the "invisible" virtual clock as an input to a test system., there is no motivation to modify the teachings of Selvidge with the teachings of Dargelas, and claims 22, 28, and 34 are patentable over the cited combination of references.

For each of the foregoing reasons, the Examiner fails to establish a prima facie case of obviousness, and claims 22, 28, and 34 are patentable over the cited combination of references. Their respective dependent claims are likewise patentable.

With respect to claims 23, 29, and 35:

With respect to claims 23, 29, and 35, the claims recite selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

The Examiner fails to give full consideration to each element of this claim recitation. The office action cites the same portion of Selvidge, namely column 18, lines 58-65 (reproduced above). However, this analysis completely ignores the claim language of "in accordance with respective race resolution requirements of the respective sequential elements."

As previously noted, Selvidge discloses providing a virtual clock to a flip-flop to transform an implicit state into an explicit state element. However, the cited portion is silent with respect to race resolution requirements. Accordingly, the Examiner has failed to establish a prima facie case of obviousness and claims 23, 29, and 35 are separately patentable for at least that reason.

Applicants further note that at most the cited portion describes providing a single flip-flop 1602 to transform a single state element. Accordingly, the cited portion does not read on the recited respective elements with respective race resolution requirements.

Applicants further note that the office action purports to disagree with applicants arguments in numbered paragraph 6-3, but the office action fails to offer any rebuttal which is readily apparent to be pertinent to these claims recitations.

With respect to claims 24, 30, and 36:

Claims 24, 30, and 36 each recite features related to the virtual clock signal being identified as a primary input of an automatic test pattern generation (ATPG) system. The cited combination of references fails to teach or suggest these claim recitations.

The office action asserts that Dargelas discloses "the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system." This is factually inaccurate as is evidenced by a review of the cited portion of Dargelas, which is silent with respect to virtual clock signals. As has been previously pointed out and as remains unrefuted, Dargelas makes no mention of virtual delay elements or virtual clocks. In the absence of a factually accurate statement of the relevant teachings of Dargelas, the Examiner has failed to establish a prima facie case of obviousness.

As noted above, Selvidge teaches that the virtual clock signal is invisible to the environment. Accordingly, one of ordinary skill in the art would not be motivated to provide the 'invisible' virtual clock signal of Selvidge as a primary input of an ATPG system. Moreover, even in the cited portion of Dargelas, Dargelas distinguishes between primary input clock signals and internal clock signals. Assuming for the sake of argument that the references may be combined in some fashion, the virtual clock signal of Selvidge at most might correspond to an internal clock signal in Dargelas, but would not correspond to a primary input.

Because Dargelas fails to teach or suggest the virtual clock signal being identified as a primary input of an automatic test pattern generation (ATPG) system, and because Selvidge teaches away from the combination, and because one of ordinary skill in the art would not be motivated to make the modification proposed, the Examiner has failed to establish a prima facie case of obviousness and claims 24, 30, and 36 are separately patentable.

Claims 25, 31, and 37:

With respect to claims 25, 31, and 37, the claims recite that the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit. The portion of Selvidge relied upon by the Examiner, namely col. 18, lines 65-67, describes a logical characteristic of the circuit, not a physical characteristic. For the Examiner's convenience the cited portion is reproduced below:

Additional virtual clock cycles are required for the values in the
loop to settle into their final states.

The cited portion is silent with respect to any physical characteristic of the circuit.
Accordingly, the office action fails to establish a prima facie case and claims 25, 31, and
37 are separately patentable for at least that reason.

Moreover, the Examiner is completely missing the point. The virtual clock in
Selvidge is not specified in accordance with any characteristic, physical or otherwise, of
the circuit described in the cited portion at col. col. 18, lines 65-67. Rather, the virtual
clock in Selvidge is simply specified to be a fixed frequency clock signal at a much
higher frequency than the true clock of the circuit. Selvidge describes how the virtual
clock is specified in connection with Fig, 4B, at col. 8, lines 6-15.

Claims 26, 32, and 38:

With respect to claims 26, 32, and 38, these claims depend from claims 25, 31,
and 37, respectively and recite that the physical characteristic comprises a delay
characteristic. Read together with their base claims, the claims recite that the virtual
clock signal is specified by a user of the ATPG system in accordance with a physical
characteristic of the circuit, wherein the physical characteristic comprises a delay
characteristic.

The delay "period" described in col. 19, lines 1-14 of Selvidge does appear to
correspond to any physical characteristic of the circuit, but rather only to a number of
simulation cycles required for logical states to settle. In any event, the VClk described in
Selvidge is not specified in accordance with the identified delay "period." Accordingly,
the office action fails to establish a prima facie case and claims 26, 32, and 38 are
separately patentable for at least that reason.

As noted above, the virtual clock in Selvidge is simply specified to be much faster
than the true clock, and not in accordance with any delay characteristic of the circuit

described at col. 19, lines 1-14. Applicants further note that the additional cycles to settle described in Selvidge are in fact an artifact of the state control element (flip-flop 1602) being inserted in the loop, and are not related to any characteristic, physical, delay, or otherwise, of the circuit.

With respect to claims 27, 33, and 39:

With respect to claims 27, 33, and 39, the claims recite that the delay characteristic corresponds to a length of conductive paths between circuit elements.

The nested loops described in col. 19, lines 1-14 of Selvidge relate only to the logical structure and not the physical structure. The cited portion is devoid of any description related to lengths of conductive paths. Accordingly, the office action fails to establish a prima facie case and claims 27, 33, and 39 are separately patentable for at least that reason.

In numbered paragraph 6-6, the Examiner argues that 'nested loops and more clock cycles indicate delay characteristics associated with loops which are related to the length of conductive paths.' Applicants note that this statement finds no basis in the prior art of record. Selvidge is simply not directed to and does not describe the physical characteristics of the circuits. The Examiner's position, particularly with respect to the specific recitation of 'a length of conductive paths,' is simply untenable.

New claims 40, 41, and 42

The new claims are directed to further feature not taught or suggested by the prior art of record, and are believed to be patentable. The new claims are supported at least by Fig. 3A and the related description on page 6, line 28 through page 7, line 4. No new matter has been added.
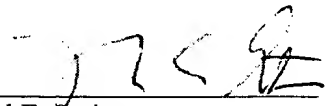
In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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